AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 3, line 4, with the following rewritten paragraph:

In order to relax electric field effect concentration on the boundary between the electric field relaxation layer and source·drain regions, thereby ~~dissolving~~ solving one of the above-described problems, a structure, as illustrated in FIG. 41, of covering the source·drain regions 17,18 with the electric field relaxation layers 9,8 was investigated. The problem, that is, lowering in breakdown voltage due to breakage of the gate insulating film 5 at the end portions of the gate electrode has not yet been ~~dissolved~~ solved.

Please replace the paragraph beginning at page 3, line 13, with the following rewritten paragraph:

An improvement in breakdown voltage by disposing a field oxide film 4a at the end portions of the gate electrode FG as illustrated in FIG. 42 was investigated, ~~failing~~ but failed to relax electric field effect concentration on the boundary between the electric field relaxation layers 9,8 and source·drain regions 17,18.

Please replace the paragraph beginning at page 4, line 12, with the following rewritten paragraph:

Among the ~~inventions~~ aspects of the invention disclosed by the present application, ~~outline of the typical~~ some principal ones will next be described.

Please replace the paragraph beginning at page 15, line 13, with the following rewritten paragraph:

A manufacturing method of a semiconductor integrated circuit device according to this Embodiment will be described in the order of steps based on FIGS. [[11]] 1 to [[22]] 22(b).

Please replace the paragraph beginning at page 15, line 16, with the following rewritten paragraph:

First, a semiconductor substrate 1 made of p type single crystal silicon as illustrated in FIG. 1 is prepared. This semiconductor substrate 1 has a region LN wherein a low breakdown voltage n channel type MISFETQn1 is to be formed, a region LP wherein a low breakdown voltage p channel type MISFETQp1 is to be formed, a region HN wherein a high breakdown voltage n channel type MISFETQn2 is to be formed, a region HP wherein a high breakdown voltage p

channel type MISFETQp2 is to be formed and a region CA wherein a ~~capacitative~~ capacitive element C is to be formed.

Please replace the paragraph beginning at page 17, line 3, with the following rewritten paragraph:

As illustrated in FIG. 4, a resist film R2 is formed over the low breakdown voltage n channel type MISFET forming region LN, low breakdown voltage p channel type MISFET forming region LP and high breakdown voltage p channel type MISFET forming region HP. With this resist film R2 as a mask, ion implantation of boron is conducted. The ion implanting energy at this time is set so that boron is also implanted below the field oxide films 4,4a in the high breakdown voltage n channel type MISFET forming region HN and ~~capacitative~~ capacitive element forming region CA. After removal of the resist film R2, an n type isolation region 6 (n type well 6) and a p type well 7 are formed by heat treatment at 1200°C (FIG. 5). In this Embodiment, the p type well 7 is formed below the field oxide films 4,4a in the ~~capacitative~~ capacitive element forming region CA, but instead, another n type well 6 may be formed.

Please replace the paragraph beginning at page 19, line 20, with the following rewritten paragraph:

As illustrated in FIG. 8, a resist film R6 is formed over a region other than the low breakdown voltage n channel type MISFET forming region LN. With this resist film R6 as a mask, boron is ion-implanted, followed by heat treatment, whereby a p type well 8b is formed (FIG. 9). Upon this ion implantation, a p type well 8c may be formed by ion implantation of ~~born~~ boron below the field oxide film 4 in the high breakdown voltage n channel type MISFET forming region HN. This p type well 8c is formed, similar to the n type well 9c, to raise the threshold voltage Vt of a parasitic MOS formed over the field oxide film 4.

Please replace the paragraph beginning at page 21, line 1, with the following rewritten paragraph:

As illustrated in FIG. 11(a), the silicon oxide film 5b is patterned to leave the silicon oxide film 5b over the field oxide film 4 in future gate electrode regions of the high breakdown voltage MISFETQn2,Qp2, the high breakdown voltage n channel type MISFET forming region HN, the high breakdown voltage p channel type MISFET forming region HP and the ~~capacitative~~ capacitive element forming region CA.

By this treatment, the silicon oxide film 5b is not left over the field oxide film 4 (except for the boundary between the high breakdown voltage region and the low breakdown voltage region, that is, in FIG. 11(a), a region of the field oxide film 4 on the boundary of the high breakdown voltage n channel type MISFET forming region HN and low breakdown voltage p channel type MISFET forming region LP) in the low breakdown voltage n channel type MISFET forming region LN and low breakdown voltage p channel type MISFET forming region LP. The silicon oxide film 5b is left over the field oxide film 4 in the ~~capacitative~~ capacitive element forming region CA so as to reduce a parasitic capacitance with the substrate (p type well 7).

Please replace the paragraph beginning at page 22, line 12, with the following rewritten paragraph:

As illustrated in FIG. 11(b), the silicon oxide film 5b is also removed from the semiconductor region (fourth semiconductor region) over the semiconductor region 9d or 8d for feeding the n type isolation region 6 or p type well 7 with a power supply voltage or ground level voltage (fixed potential) ~~(an opening portion as described in~~

~~claim)~~. This semiconductor region 9d or 8d has the same conductivity type as that of the n type isolation region 6 or p type well 7 wherein it is formed. At least one semiconductor region 9d or 8d is formed inside of the n type isolation region 6 or p type well 7 and to it, a power supply voltage and or ground level voltage ~~are~~ is applied.

Please replace the paragraph beginning at page 23, line 20, with the following rewritten paragraph:

Owing to the silicon oxide film 5c over the field oxide film 4 in the high breakdown voltage n channel type MISFET forming region HN, high breakdown voltage p channel type MISFET forming region HP and ~~capacitative~~ capacitive element forming region CA, the threshold voltage Vt of a parasitic MOS formed over these regions can be heightened.

Please replace the paragraph beginning at page 24, line 17, with the following rewritten paragraph:

As illustrated in FIG. 14(a), the polycrystalline silicon film 10 is then patterned to leave it on the gate insulating film 5 (5a,5c) of the high breakdown voltage MISFETQn2,Qp2. This polycrystalline silicon film 10 is to be a gate electrode FG (first conductive film) of the high

breakdown voltage MISFETQn2,Qp2. At this time, the polycrystalline silicon film 10 is left also on the silicon oxide film 5c of the ~~capacitative~~ capacitive element forming region CA (third region). This polycrystalline silicon film 10 is to be a lower electrode LE of the ~~capacitative~~ capacitive element C. Here, the gate electrode of each of the high breakdown voltage MISFETQn2,Qp2 is formed from the polycrystalline silicon film 10 (FG), but as will be described later, the gate electrode of each of the high breakdown voltage MISFETQn2,Qp2 may be formed from a polycrystalline silicon film 11 (SG) which will be described later. FIG. 14(b) and FIG. 16(b) ~~each illustrates~~ illustrate the case wherein the gate electrodes of the high breakdown voltage MISFETQn2,Qp2 are formed from the polycrystalline silicon film 11.

Please replace the paragraph beginning at page 25, line 21, with the following rewritten paragraph:

As illustrated in FIG. 16(a), after removal of the thin silicon oxide film 5a over the low breakdown voltage n channel type MISFET forming region LN and low breakdown voltage p channel type MISFET forming region LP, a silicon oxide film to be a gate insulating film 5d (fourth

insulating film) of the low breakdown voltage MISFETQn1,Qp1 is formed by thermal oxidation. At this time, the gate electrode FG of each of the high breakdown voltage MISFETQn2,Qp2 is slightly oxidized. The surface of the lower electrode LE is also slightly oxidized and a silicon oxide film (not illustrated) is formed thereover. This silicon oxide film serves as a ~~capacitative~~ capacitive insulating film. Alternatively, after deposition of the polycrystalline silicon film 10 which will be the lower electrode LE, a silicon nitride film may be formed in advance over this polycrystalline silicon film 10 as a ~~capacitative~~ capacitive insulating film in order to improve reliability of the ~~capacitative~~ capacitive element C.

Please replace the paragraph beginning at page 27, line 10, with the following rewritten paragraph:

Over the semiconductor substrate 1, a polycrystalline silicon film 11 is then deposited by CVD. This polycrystalline silicon film 11 is patterned to leave it over the gate insulating film 5d of the low breakdown voltage MISFETQn1,Qp1. This polycrystalline silicon film 11 is to be a gate electrode SG (second conductive film) of the low breakdown voltage MISFETQn1,Qp1. At this time, the

polycrystalline silicon film 11 is left also over the ~~capacitative~~ capacitive insulating film (not illustrated) over the lower electrode LE of the ~~capacitative~~ capacitive element forming region CA. This polycrystalline silicon film 11 is to be an upper electrode UE of the ~~capacitative~~ capacitive element C. Alternatively, the gate electrode SG may be formed by patterning a tungsten silicide layer formed over the surface of the polycrystalline silicon film 11. This tungsten silicide layer is formed by depositing a metal film such as tungsten film over the polycrystalline silicon film 11, followed by heat treatment. This silicide layer is formed to lower the resistance of the gate electrode SG.

Please replace the paragraph beginning at page 28, line 4, with the following rewritten paragraph:

~~In the next place~~ Next, source·drain regions of the low breakdown voltage MISFETQn1,Qp1 and high breakdown voltage MISFETQn2,Qp2 are formed. A description will ~~next~~ be made of the formation of these source·drain regions.

Please replace the paragraph beginning at page 29, line 17, with the following rewritten paragraph:

As illustrated in FIG. 21, a resist film R10 is then formed over the low breakdown voltage n channel type MISFET forming region LN, and the gate electrode FG of each of the high breakdown voltage n channel type MISFET forming region HN and high breakdown voltage p channel type MISFETQp2. With this resist film R10 as a mask, boron is ion-implanted, followed by annealing and activation, whereby p^+ type semiconductor regions 18 (source·drain regions) are formed on both sides of each of the gate electrodes (SG,FG) of the low breakdown voltage p channel type MISFETQp1 and high breakdown voltage p channel type MISFETQp2 (FIG. 22(a)). At this time, boron is not implanted below the ~~filed~~ field oxide films 4,4a and silicon oxide film 5c.

Please replace the paragraph beginning at page 32, line 11, with the following rewritten paragraph:

By these steps, the gate electrode of each of the low breakdown voltage MISFETQn1,Qp1 and high breakdown voltage MISFETQn2,Qp2 can be formed simultaneously from the polycrystalline silicon film 11 (SG). The gate electrode of each of the low breakdown voltage MISFETQn1,Qp1 and high breakdown voltage MISFETQn2,Qp2 may also be formed from the polycrystalline silicon film 10, but if so, the

polycrystalline silicon film 11 inevitably remains over the side walls of the gate electrode in the subsequent deposition and patterning steps of the polycrystalline silicon film 11, which adversely affects the characteristics of MISFET. It is therefore ~~desired~~ preferred to form these gate electrodes from the polycrystalline silicon film 11.

Please replace the paragraph beginning at page 33, line 17, with the following rewritten paragraph:

By oxidizing the surface of this semiconductor substrate 1, a silicon oxide film 2 is formed. After selective formation of a silicon nitride film 3 over this silicon oxide film, with this silicon nitride film 3 as a mask, the semiconductor substrate 1 is etched to form ~~a groove~~ grooves U of about 300 nm depth as illustrated in FIG. 24. In the high breakdown voltage MISFETQn2,Qp2 forming regions (HN,HP), a groove is formed below both ends of a gate electrode which will be described later.

Please replace the paragraph beginning at page 34, line 9, with the following rewritten paragraph:

As illustrated in FIG. 25, the silicon oxide film 104 is deposited over the substrate 1 including the inside of the groove by CVD. With the silicon nitride film [[103]] 3 as a stopper, the silicon oxide film 104 over the groove is chemically and mechanically polished to planarize its surface. By removal of the silicon nitride film 3, the silicon oxide film 104 for element isolation and the silicon oxide film 104a for improving the breakdown voltage of the high breakdown voltage MISFETQn2,Qp2 are completed (FIG. 26(a)).

Please replace the paragraph beginning at page 34, line 19, with the following rewritten paragraph:

Here, as illustrated in FIG. 26(b), a recess phenomenon of the surface of each of the silicon oxide films 104,104a at the end portion of the groove occurs owing to the above-described polishing, washing of the surface of the semiconductor substrate in a subsequent impurity implantation step or removal of the thin oxide film 2 prior to the formation of the silicon oxide film 5a. This recess phenomenon leads to various problems such as deterioration in the breakdown voltage of MISFET and occurrence of kink phenomenon as will be described below in

detail. In the ~~below~~ drawings, recess of the surface of the silicon oxide films 104,104a is not illustrated in order to simplify them.

Please replace the paragraph beginning at page 35, line 7, with the following rewritten paragraph:

With ~~regards~~ regard to steps similar to those of Embodiment 1 among the subsequent steps, overlapping description is avoided and only the outline is described.

Please replace the paragraph beginning at page 36, line 8, with the following rewritten paragraph:

As illustrated in FIG. 29, after removal of the thin silicon oxide film 2 on the surface of the semiconductor substrate 1, a silicon oxide film 5a to be a portion of a gate insulating film 5 is formed by thermal oxidation. A silicon oxide film 5b is then deposited over the semiconductor substrate 1 by low pressure chemical vapor deposition. This silicon oxide film 5b is then patterned to leave it over the silicon oxide film 104 in a future gate electrode region of the high breakdown voltage MISFETQn2,Qp2, the high breakdown voltage n channel type MISFET forming region HN and high breakdown voltage p

channel type MISFET forming region HP. The silicon oxide film 5b is not left over the silicon oxide film 104 (except for the boundary between the high breakdown voltage region and the low breakdown voltage region, that is, in this diagram, the field oxide film on the boundary of the high breakdown voltage n channel type MISFET forming region HN and low breakdown voltage p channel type MISFET forming region LP) ~~over~~ in the low breakdown voltage n channel type MISFET forming region LN and low breakdown voltage p channel type MISFET forming region LP. Since the silicon oxide films 104 over these regions are narrow as described in Embodiment 1, ~~so that~~ such a structure is adopted in order to prevent narrowing of the width of each of the source·drain regions or gate electrode of MISFETQn1,Qn2 due to mask misalignment.

Please replace the paragraph beginning at page 42, line 20, with the following rewritten paragraph:

As illustrated in FIG. 35, after removal of the thin silicon oxide film 5a over the low breakdown voltage n channel type MISFET forming region LN and low breakdown voltage p channel type MISFET forming region LP, a gate insulating film 5d of each of the low breakdown voltage

MISFETQn1,Qp1 is formed by thermal oxidation. At this time, a gate electrode FG of each of the high breakdown voltage MISFETQn2,Qp2 is slightly oxidized (5e). The surface of a lower electrode (LE) is also oxidized slightly, whereby a silicon oxide film (5f) is formed (FIG. 35). This silicon oxide film 5f serves as a ~~capacitative~~ capacitive insulating film of the ~~capacitative~~ capacitive element C. Alternatively, it is also possible to form in advance a silicon nitride film over a polycrystalline silicon film 10, which has been deposited as a lower electrode LE, and use it as a ~~capacitative~~capacitive insulating film.

Please replace the paragraph beginning at page 45, line 17, with the following rewritten paragraph:

Over the polycrystalline silicon film 111, a polycrystalline silicon film 111b is then deposited. These polycrystalline silicon films 111,111b are to be gate a electrode SG of each of the low breakdown voltage MISFETQn1,Qp1. These polycrystalline silicon films 111,111b are therefore patterned to leave them over the gate insulating film 5d (FIG. 38). At this time, the polycrystalline silicon films 111,111b are also left over a

silicon oxide film 5f over the lower electrode LE of the ~~capacitative~~ capacitive element forming region CA. These polycrystalline silicon films 111,111b are to be an upper electrode UE of the ~~capacitative~~ capacitive element C. Alternatively, the gate electrode SG may be formed by forming a tungsten silicide layer over the surface of the polycrystalline silicon film 111b, followed by patterning. This tungsten silicide layer is formed by depositing a metal film such as tungsten over the polycrystalline silicon film 111 and heat treating it. This silicide layer is formed to reduce resistance of the gate electrode SG.

Please replace the paragraph beginning at page 48, line 22, with the following rewritten paragraph:

Advantages available ~~by the~~ with typical ~~inventions, among the inventions disclosed by~~ implementations of the present ~~application,~~ invention will next be described simply.